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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,367	09/28/2000	Francis X. McKeen	042390.P9578	7649

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EXAMINER	
HO, THOMAS M	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,367	MCKEEN ET AL.	
	Examiner	Art Unit	
	Thomas M. Ho	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/2/04, 6/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending.

Response to Arguments

2. In view of the Appeal Brief filed on 2/16/06, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Objections

3. Claim 3 recites "when a graphics card is in isolated execution mode" however, claims 1 and 2, which claim 3 is dependent on do not recite that a graphics card is in isolated execution mode, but rather that a processor is in isolated execution mode. While graphics cards often contain processors, it is noted that a graphics card itself is not a processor, nor can a processor be said to be equivalent to a processor as understood in the art.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1, 2, 7-10, 12, 13, are rejected under 35 USC § 101 the claimed invention lacks patentable utility.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result."

Claims 1, 2, 7-10, 12, 13 are not limited to producing a tangible result. Instead they appear to merely recite the execution of a particular processing mode. A tangible operating result however is not recited by these claims.

For example, in reference to claim 12, the Applicant has recited:

A method comprising:

Establishing an isolated execution environment having an isolated execution mode; and

preventing access to output data by any requester not operating in an isolated mode.

No tangible result however has been produced. Instead, an isolated environment for execution has been established, and access to output data has been prevented. However the claim itself lacks utility because such a result is not useful, concrete, and tangible. MPEP 2106 II A

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 2, 7-10, 12, 13 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the relationships between the constituent components to perform the actions of the claims.

For Example claim 1 recites a processor executing in normal mode and an isolated mode. Additionally, claim 1 recites a system memory including isolated areas, and an output device.

No linkage between these claimed elements is recited however. The essential steps in which each of these components interact with each other is not recited in the claims. No disclosure towards their interrelating interactions or how they interoperate is given.

Claims 12 and 13 suffer from the deficiency that no steps are recited as to how the isolated execution environment is established or what operations are performed in order to achieve the step of preventing access to output data by any requestor not operating in isolated mode. No disclosure of the interrelating elements of operation is given to achieve these steps.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 6, 12, 13, 15, 16, 19-22 rejected under 35 U.S.C. 102(e) as being anticipated by England et al., US patent 6775779.

In reference to claim 1:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode, where the processor can execute in different modes and the isolated execution mode is the secure mode of execution. (Column 5, lines 35-55)
- A system memory (Figure 1, Item 140, 141) including an isolated area, an isolated output area, and a non-isolated area, where the system memory is divided into rings of isolation or protection. (Figure 2) & (Column 5, line 55 – Column 6, line 12)
- An output device, where the output device is an I/O adaptor that may be a monitor, video card frame buffer or sound card. (Figure 1, Item 170, 172) & (Column 4, line 40-55) & (Column 13, lines 1-50)

In reference to claim 6:

England et al. discloses the platform of claim 1 further comprising:

- An operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode, where the operating system provides a secure operating environment and wherein the secure mode involves input/output conversions. (column 5, lines 13-35)

In reference to claim 12:

England et al discloses a method comprising: (Column 7, lines 50-56) & (Column 12, line 25-Column 13, line 50) & (Column 8, line 25-52)

- Establishing an isolated execution environment having an isolated execution mode, where the isolated execution environment is an secure execution mode.
- Preventing access to output data by any requester not operating in an isolated mode, where the output area where output data is written to is protected from external modification or access.

In reference to claim 13:

England et al. discloses the method of claim 12 wherein establishing comprises:

- Segregating a system memory into an isolated output area and a non-isolated area. (Figure 2) & (Column 5, lines 55 – Column 6, line 32)

In reference to claim 15:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 13 wherein preventing comprises:

- Identifying if an isolated attribute is present in a request for access to the requested output area, where the isolated attribute is a CC code attached to requests to indicate it is part of the secure operating mode. And Denying the request if no isolated attribute is present, where the attribute is denied if no CC code is found, or it is improper.

In reference to claim 16:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 13 further comprising:

- Loading data from the isolated output area into a bit plane on a graphics card, where the bit plane is the frame buffer.
- Denying all external access to the bit plane, where external access is denied by unauthorized access attempts.

In reference to claim 19:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode; (Column 5, lines 35-55)
- A direct memory access controller to issue requests for access to an isolated output area; (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52)
- A first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52)
- A second interface coupled to the DMA controller to supply output data to an output device. (Figure 1, Item 171, 172) & (Column 4, lines 40-55)

In reference to claim 20:

England et al. discloses the apparatus of claim 19 wherein the first interface is a secure accelerated graphics port (AGP) and the output device is a display. (Column 4, lines 15-40)

In reference to claim 21:

England et al. discloses the apparatus of claim 19 wherein the DMA controller attaches an isolated attribute to any isolated output area access request, where the isolated attribute is a CC code. (Column 6, lines 19-65) & (Column 7, lines 50-56)

In reference to claim 22:

England et al. discloses the apparatus of claim 19 wherein the second interface is an audio interface. (Column 4, lines 40-55) & (Column 13, lines 20-50)

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-5, 7-11, 14, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. US patent 6775779.

In reference to claim 2:

England et al. fails to explicitly disclose the platform of claim 1, wherein the output device is a graphics card.

England et al. however teaches a method of protecting content through a method of secure processor modes combined with secure memories. (Abstract) & Figure 2)

England et al. additionally discloses that among this content, there may be audio and video content. It is further disclosed that access to these modules and drivers by requests external to the secure mode are restricted. (Column 2, lines 5-15) & (Column 2, line 65 – Column 3, line 10)

England et al. further discloses that the hardware components used may include that which is standard to a conventional PC. (Column 4, lines 15-40) and among the I/O devices that may serve as the isolated output area includes frame buffers. (Column 13, lines 1-50)

A search of the prior art has uncovered that PC frame buffers are frequently called graphics cards.

Framebuffer

From Wikipedia, the free encyclopedia
*(Redirected from **Frame buffer**)*
*Jump to: **navigation**, **search***

*The **framebuffer** is a video output device that drives a video display from a memory buffer containing a complete **frame** of data. The information in the buffer typically consists of color values for every **pixel** (point that can be displayed) on the screen. Color values are commonly stored in 1-bit **monochrome**, 4-bit **palletized**, 8-bit **palletized**, 16-bit **highcolor** and 24-bit **truecolor** formats. An additional **alpha channel** is sometimes used to retain information about pixel transparency. The total amount of the memory required to drive the framebuffer is dependent on the **resolution** of the output signal, as well as the **color depth** and **palette** size.*

*Framebuffers differ significantly from the **vector graphics displays** that were common prior to the advent of the framebuffer. With a vector display, only the **vertices** of the graphics primitives are stored. The electron beam of the output display is then commanded to move from vertex to vertex, tracing an analog line across the area between these points. With a framebuffer, the electron beam (if the display technology uses one) is commanded to trace a left-to-right, top-to-bottom path across the entire screen, much in the same way a television renders a broadcast signal. The color information for each point on the screen is then pulled from the framebuffer, creating a set of discrete picture elements (**pixels**).*

*(**PC** framebuffers are commonly referred to as "Graphics Cards"), many users assume that a framebuffer is simply an area of memory for storing graphics.*

Although England et al. does not explicitly recite the limitation of a graphics card, in light of the disclosures of the prior art, it would have been obvious to one of ordinary skill in the art to use graphics cards as part of the isolated output area, where the output of England et al. is written to (Column 13, lines 1-5) in order to preserve the security of secure system by regulating access to output data written to the video memory.

In reference to claim 3:

England et al. discloses the platform of claim 2 further comprising:

- A memory control hub (MCH) coupled between the system memory, and the processor and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode, where the graphics card is the video output adaptor with the frame buffer, and access to the frame

buffer output is only permitted when in the secure mode. (Column 8, lines 25-53) & (Column 12, lines 25-67) & (Column 13, lines 1-18) & (Column 13, lines 37-50) & (Column 7, lines 50-55)

In reference to claim 4:

England et al. discloses the platform of claim 3 wherein the graphics card comprises:

- A direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted, where attempts to transfer and store data from the output area to local storage such as memory is interdicted. (Column 7, lines 50-55) & (Column 13, lines 37-50)

In reference to claim 5:

England et al. discloses the platform of claim 3 wherein only the graphics card is permitted to read the isolated output area. (Column 12, lines 57-67) & (Column 13, lines 1-18) & (Column 10, lines 49-57)

In reference to claim 7:

England et al. discloses the platform of claim 3 further comprising:

A link between the graphics card and the MCH having an isolated transaction type, where the isolated transaction type is indicate by the secure CC number indication. (Column 12, lines 25-Column 13, line 15) & (Column 6, line 19-32)

In reference to claim 8:

England et al. discloses the platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area. (Column 12, line 25 – Column 13, line 50) & (Column 7, line 50-56) & (Column 8, line 25-52)

In reference to claim 9:

England et al. discloses the platform of claim 7 wherein the link is a secure accelerated graphics port bus, where the accelerated graphics port bus is an AGP port bus. (Column 4, line 15-40)

In reference to claim 10:

England et al. (column 6, lines 25-32) & (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 2 wherein the graphics card comprises:

- An isolated bit plane, where the isolated bit plane is the memory of the frame buffer in secure more.
- A non-isolated bit plane, where the non isolated bit plane is the memory of the frame buffer when in unprotected mode.

In reference to claim 11:

England et al. (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

In reference to claim 14:

England et al. discloses the method of claim 13 further comprising:

- Issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; (Column 12, lines 25 – Column 13, line 50)
- Refreshing the display based on the display data, where refreshing to display based on the display data is inherent to the function and purpose of a frame buffer. (Column 13, lines 1-15)

In reference to claim 17:

England et al. (Column 12, lines 25 – Column 13, line 50) discloses the method of claim 16 further comprising:

- Defining a first window for display of an image corresponding to the bit plane, where the window that corresponds to the bit plane is the image stored in the frame buffer that is to be rendered to the monitor.
- Occluding all windows but the first window, where the first window is the information in the frame buffer, and the non display information is occluded.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. US patent 6775779 and Cunnif et al, US patent 6476806.

In reference to claim 18:

England et al. discloses the method of claim 13 further comprising:

- Retrieving data from the isolated output area, where the value of the secure memory may be accessed to a request being in secure mode. (Column 12, lines 25 – Column 13, line 50)
- Displaying an image corresponding to the data, where displaying an image corresponding to the data is inherent to the functioning of a frame buffer.

England et al. fails to disclose :

- Occluding the image prior to a platform transitioning out of isolated execution mode.

Cunnif et al. (Column 2, lines 40-45) & (Column 5, lines 8-36) discloses a method of occluding a part of an image based on the mode of execution or a mode of the processor, and will occlude images in one mode, prior to switching to another mode.

England et al. (Column 12, lines 25 – Column 13, line 50) teaches that memory mapped IO devices such as a frame buffer should not have their information be read by untrusted software. It would have been obvious to one of ordinary skill in the art at the time of invention to occlude the image information in the frame buffer in order to prevent other non-secure software and access requests from accessing the information.

Conclusion

11. Any inquiry concerning this communication from the examiner should be directed to

Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962.

The Examiner may also be reached through email through **Thomas.Ho6@uspto.gov**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

General Information/Receptionist	Telephone: 571-272-2100	Fax: 571-273-8300
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TMH

May 15th, 2006

CHRISTOPHER REVAK
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